

Request for Quotation: ASIC SOC / Structured ASIC

Customer info

Name	
Company	
Job Title	
E-mail	
Phone	
Fax	
Address	
City	
State	
Zip/Postal Code	

Project info

Project name	
Application	
New or existing design	

*Please add some word/links about your company and target market

Commercial info

Schedule requirements (Dates)

Vendor Selection	
RTL ready	
Netlist ready	
Tape Out	
Samples Delivery	

Production Start:

Year			
Annual Volumes			
Target Unit Price			

Target NRE:

Life Span(Years):

Technical info

Preferred Process Technology:

0.35um 0.25um 0.18um 0.13um 90nm 65nm other: _____

Implementation Preference:

Standard Cell Embedded Array Gate Array Supplier Discretion

Random Gate Count (No IPs)

	FlipFlop Counts	Frequency [MHz]	Activity Rate	Combinational Logic	Frequency [MHz]	Activity Rate
1.						
2.						
3.						
Total Gate Count						

(1Gate equal to one NAND Gate)

Memory Specification

Type	Num. of Instance	Configuration Words/Bits	Sync/ Async	Activity Rate	Frequency [MHz]

*Type : eDRAM, SRAM, ROM, Flash, OTPROM, other

SP-Single Port Ram, DP-Dual Port RAM(1RW/1R, 2RW), TP-Triple Port RAM, other.

*Sync-Synchronous, ASync-ASynchronous

Maximum System Clock Speed [MHz] :

Core Voltage:

1.2V 1.8V 2.5V 3.3V 5V Other _____

Thermal Specifications

Max Power Dissipation [W]:

Operation Min to Max Ambient Temp(Celsius) :

I/O voltage:

1.2V 1.8V 2.5V 3.3V 5V 3.3/5V Tolerant Other _____

I/O specification:

Type	# of Input I/O	# of Output I/O	# of Bidir I/O	Frequanc y [MHz]	Driv e [mA]	Load [pF]	# of SSO	Total Num. of Type
Total Number of Functional I/O								
Total Number of I/O pin including Power								

*Type : CMOS/LVTTL, LVDS, HSTL, SSTL, Other

Package Preference & Size / Die Format :

* QFP, BGA, BCC other;

Analog Macro Specification: [like DAC, ADC, PLL ...]

Type	Specification	Num. of Instance

* for DAC, ADC please mention all parameters like number of bits, sampling rate etc.

* for PLL please mention all parameters like input & output frequency, duty, jitter, phase skew etc.

Digital Macro/IP Specification:

Type	Specification	Num. of Instance

Total Die Size [mmXmm]:

Design Hand-off Level:

Full Turn-Key RTL(VHDL/Verilog) Gate Level Netlist Other _____

Requested Services from Supertec :

Core Design

Synthesis

DFT : SCAN JTAG Memory Test ATPG

Formal Verification

Static Timing Analysis

Simulation & Test vectors generation

Power Analysis

Other _____

Design Tools used by Customer :

Synthesis Synopsys Cadence Other _____

DFT Synopsys Cadence Mentor Grapics Other _____

Formal Verification Synopsys Other _____

Simulation Synopsys Cadence Model Sim Other _____

STA Synopsys Other _____

Power Synopsys Cadence Other _____

Other _____

Comments :